

10/512405

05 Rec'd PCT/PTO 25 OCT 2004

26.09.03

World Intellectual Property Organization
PCT Division
34 Chemin des Colombettes
1211 Geneva 20
Switzerland

Amendment of the claims under Article 19 (1) (Rule 46)

International Application No. : PCT/JP03/04866

International Filing Date: 16.04.03

Applicant: Name SUMITOMO MITSUBISHI SILICON CORPORATION

Address 2-1, Shibaaura 1-chome, Minato-ku, Tokyo 105-0023 JAPAN

Agent: Name UBUKATA Motoshige

Address 6-15, Kawaramachi 4-chome, Chuo-ku, Osaka-shi, Osaka 541-0048 Japan

Telephone number 06-6201-3851

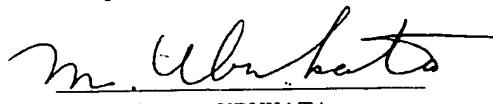
Dear sir

The Applicant, who received the International Search Report relating to the above identified International Application transmitted on 16. 04. 03, hereby files amendment under Article 19 (1) as in the attached sheets.

The filing sheets of amendment under Article 19 (1) are change of papers, which are pages (page 45, 46, 47) written 「Claims」 in the above identified International Application. Herein, claims 7 and 17 are amended, other claims 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15 and 16 are retained unchanged.

The Applicant also files as attached herewith a brief statement explaining the amendment.

Very truly yours,


Motoshige UBUKATA

Attachment:

(1) Amendment under Article 19(1)	1 sheet
(2) Brief Statement	1 sheet

arguiae
Pages 69-73
Replaced by
Article 19 and
Amend

CLAIMS

1. A high-resistance silicon wafer having resistivity of $100 \Omega\text{cm}$ or more, wherein an oxygen precipitate (BMD) having a size of $0.2 \mu\text{m}$ or more is formed so as to have density of $1 \times 10^4/\text{cm}^2$ in the wafer, an oxygen concentration in the wafer is $12 \times 10^{17} \text{ atoms/cm}^3$ (ASTM F-121, 1979) or less, and carbon concentration is $0.5 \times 10^{16} \text{ atoms/cm}^3$ or more.

2. The high-resistance silicon wafer according to claim 1, wherein a density of a LPD (Light Point Defect) having a size of $0.12 \mu\text{m}$ or more and observed on a surface of the wafer is controlled so as to be $0.2/\text{cm}^2$ or less.

3. A high-resistance silicon wafer having resistivity of $100 \Omega\text{cm}$ or more, wherein a density of a grown-in defect detected by seco etching is $1 \times 10^3/\text{cm}^3$ or less, an oxygen precipitate (BMD) having a size of $0.2 \mu\text{m}$ or more is formed so as to have density of $1 \times 10^4/\text{cm}^2$ or more in the wafer and an oxygen concentration in the wafer is $12 \times 10^{17} \text{ atoms/cm}^3$ (ASTM F-121, 1979) or less.

4. The high-resistance silicon wafer according to claim 3, wherein carbon concentration in the wafer is $0.5 \times 10^{16} \text{ atoms/cm}^3$ or more.

5. The high-resistance silicon wafer according to claim 1 or 3, wherein a DZ (Denuded Zone) layer is formed at least 5 μm or more in depth from a surface of the wafer.

6. The high-resistance silicon wafer according to claim 1 or 3, wherein value of oxygen concentration (ASTM F-121, 1979) of the wafer is limited in ranges of 12×10^{17} atoms/cm³ or less, 7×10^{17} atoms/cm³ or less, and 5.8×10^{17} atoms/cm³ or less when the resistivity of the wafer is not less than 100 Ωcm and less than 300 Ωcm , not less than 300 Ωcm and less than 2000 Ωcm , and not less than 2000 Ωcm , respectively.

7. A manufacturing method of a high-resistance silicon wafer, characterized in that a primary silicon wafer in which resistivity is 100 Ωcm or more, oxygen concentration is 12×10^{17} atoms/cm³ (ASTM F-121, 1979) or more, and a carbon concentration is $0.5 / 10^{16}$ atoms/cm³ or more is used, a remaining oxygen concentration in the wafer is controlled to be 12×10^{17} atoms/cm³ (ASTM F-121, 1979) or less by performing a heat treatment for forming an oxygen precipitate nucleus and a heat treatment for growing the oxygen precipitate on the primary silicon wafer.

8. A manufacturing method of a high-resistance silicon wafer, characterized in that a primary silicon wafer

in which resistivity is 100 Ωcm or more, an oxygen concentration is 14×10^{17} atoms/cm³ (ASTM F-121, 1979) or more, and a density of a grown-in defect detected by secondary ion mass spectrometry (SIMS) is $1 \times 10^3/\text{cm}^3$ is used, a remaining oxygen concentration in the wafer is controlled to be 12×10^{17} atoms/cm³ (ASTM F-121, 1979) or less by performing a heat treatment for forming an oxygen precipitate nucleus and a heat treatment for growing the oxygen precipitate on the primary silicon wafer.

9. The manufacturing method of the high-resistance silicon wafer according to claim 7 or 8, wherein the heat treatment for forming the oxygen precipitate nucleus is a low-temperature heat treatment performed at 500 to 900°C for 5 hours or more.

10. The manufacturing method of the high-resistance silicon wafer according to claim 9, wherein the conditions of the low-temperature heat treatment is at 700 to 900°C for 5 hours or more.

11. The manufacturing method of the high-resistance silicon wafer according to claim 7 or 8, wherein the heat treatment for growing the oxygen precipitate is a high-temperature heat treatment performed at 950 to 1050°C for 5 hours or more.

for 10 hours or more.

12. The manufacturing method of the high-resistance silicon wafer according to claim 7 or 8, characterized in that an oxygen outward diffusion heat treatment is performed on the wafer at 1100 to 1250°C for 1 to 5 hours before the heat treatment for forming the oxygen precipitate nucleus.

13. The manufacturing method of the high-resistance silicon wafer according to claim 12, characterized in that the oxygen outward diffusion heat treatment is performed in a gas atmosphere containing nitrogen gas.

14. The manufacturing method of the high-resistance silicon wafer according to claim 12, characterized in that the oxygen outward diffusion heat treatment is performed in an atmosphere of a hydrogen gas, argon gas or mixed gas of these.

15. The manufacturing method of the high-resistance silicon wafer according to claim 7 or 8, characterized in that a rapid thermal annealing process is performed on the wafer before the heat treatment for forming the oxygen precipitate nucleus.

16. The manufacturing method of the high-resistance silicon wafer according to claim 15, wherein the conditions of the rapid thermal annealing process is 1150 to 1300°C for 1 to 60 seconds in an atmosphere containing nitrogen.

17. The manufacturing method of the high-resistance silicon wafer according to claim 8, wherein a carbon concentration in the primary silicon wafer is $0.5 /10^{16}$ atoms/cm³ or more.